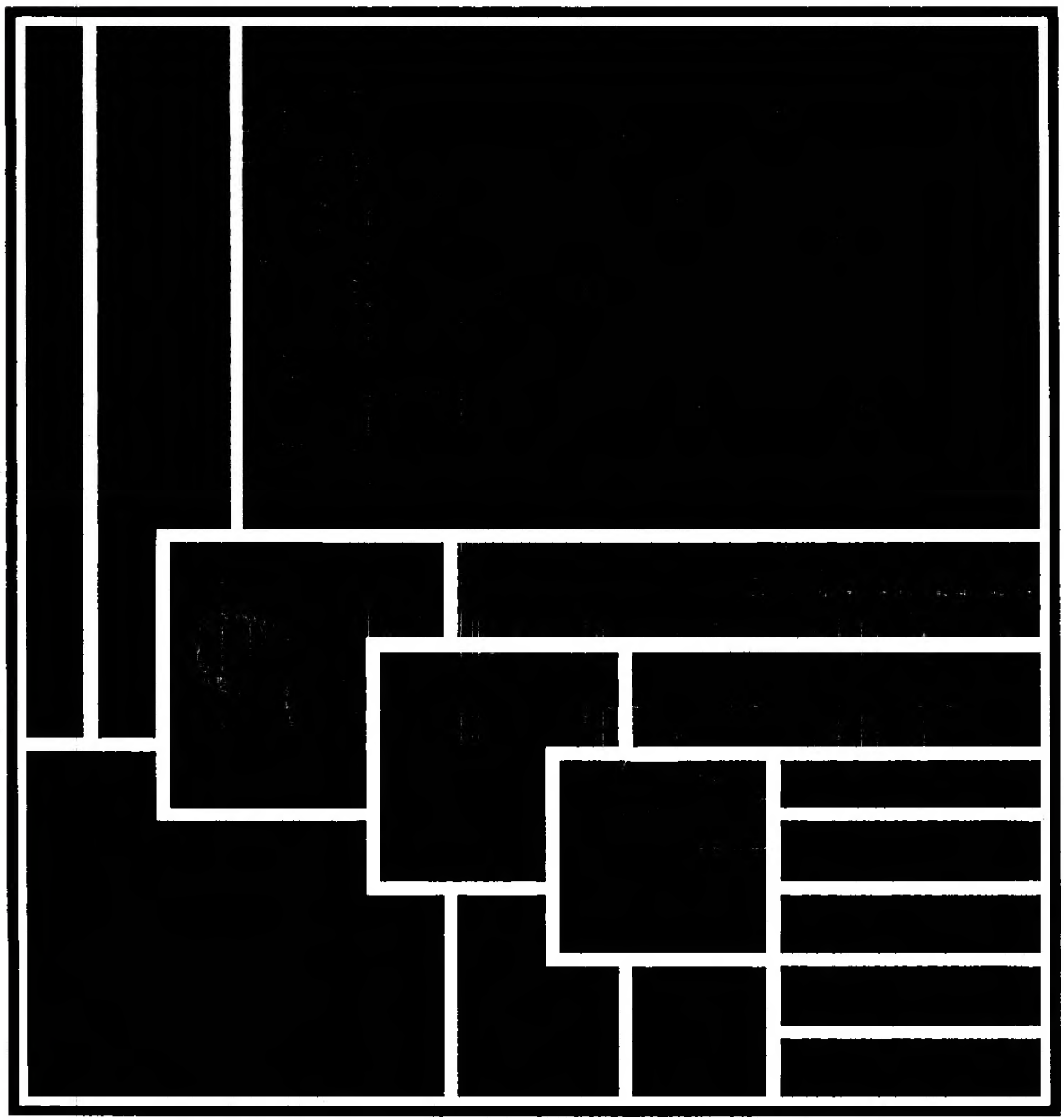
HP Computer Systems

HP 98628A/98691A
Datacomm Interface Installation



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HP 98628A/98691A
Datacomm Interface Installation

for HP Series 200 Computers

Manual Part No. 98628-90001

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Chapter 1
General Information

Introduction

The HP 98628A Data Communications Interface and HP 98691A Programmable Datacomm Interface are microprocessor-based datacomm interfaces designed for use with HP Series 200 computers. Each interface contains a built-in microprocessor and associated circuits that perform all protocol management and signalling functions for data communications using RS-232C and RS-449 connections.

The HP 98628A Datacomm Interface supports two protocols:

- Asynchronous (Async) protocol commonly used for timesharing and remote host computer applications as well as connections to remote terminals.
- HP DSN/Data Link Protocol most commonly used with Data Link network applications based around an HP 1000 network host computer.

The HP 98691A Programmable Datacomm Interface is designed for installing custom protocols or protocols that are designed and supported by suppliers other than Hewlett-Packard Company. This interface is usually sold through the supplier of the custom protocol firmware.

Several cable options are also available, accommodating most popular interconnections to standard datacomm links and modems. They are discussed in Chapter 3.

Unpacking and Inspection

If the shipping carton is damaged, ask the carrier's agent to be present when the interface is unpacked. If the interface is damaged or fails to operate properly, notify the carrier, and the nearest HP Sales and Service Office immediately if your interface is an HP 98628. Retain the shipping carton for the carrier's inspection. The sales and service office will arrange for the repair or replacement of your interface without waiting for the claim against the carrier to be settled. If your interface is an HP 98691 Programmable Datacomm Interface, contact the interface supplier for assistance in repair or replacement.

Handling

Precautionary measures should be taken to protect interface printed circuit assemblies from static discharge during handling. Each interface is shipped in a protective anti-static bag which provides adequate anti-static protection for the interface as long as it remains inside the bag. It is good practice to use additional anti-static protection, such as commercially available personnel grounding straps when servicing or installing interfaces, memory boards, and other assemblies that may be sensitive to electro-static discharge.

Avoid touching integrated circuit leads while picking up or handling the interface. Static discharge through the leads can easily destroy sensitive components. Handle the board by the card edges or metal backplane cover plate. Do NOT handle the interface by its backplane edge connector. If the edge connector inadvertently gets dirty, it can be cleaned by using a cotton swab and isopropyl alcohol.

Technical Specifications

Product Description

The HP 98628A and 98691A are microprocessor-based (Zilog Z-80A or equivalent) data communications interfaces that fit the I/O backplane of HP Series 200 computers. The interface includes on-board read-write (RAM) memory for buffering and other needs. The microprocessor performs protocol management and other data communication functions, freeing the mainframe processor for other tasks. Protocol(s) supported by the interface depend on what programs are stored in the Program ROM that is plugged into the socket on the interface card.

Physical Description

Size: 135 mm by 170 mm (5.3 in by 6.6 in)
Weight: 310 grams (11 ounces)

Environmental Range

Temperature: 0°C to 45°C (32 to 113°F)
Humidity: 0 to 80% non-condensing

Electrical Specifications

98628A power consumption (typical)

+5 V @ 710 mA
+12 V @ 37 mA
−12 V @ 60 mA

The following adapters also obtain power through the HP 98628 interface. Their consumption should be added to the interface power consumption when they are used. Typical values are shown.

HP 13264A Data Link Adapter:

+5 V @ 30 mA
+12 V @ 160 mA
−12 V @ 23 mA

HP 13265A Modem:

+5 V @ 100 mA
+12 V @ 45 mA
−12 V @ 45 mA

HP 13266A Current Loop Adapter:

+5 V @ 200 mA
+12 V @ 90 mA
−12 V @ 80 mA

Electrical Interface Compatibility (with appropriate cables)

RS-232C (similar to CCITT V.24/V.28)
RS-449/RS-423 (similar to CCITT V.10)
RS-449/RS-422 (similar to CCITT V.11)[1]

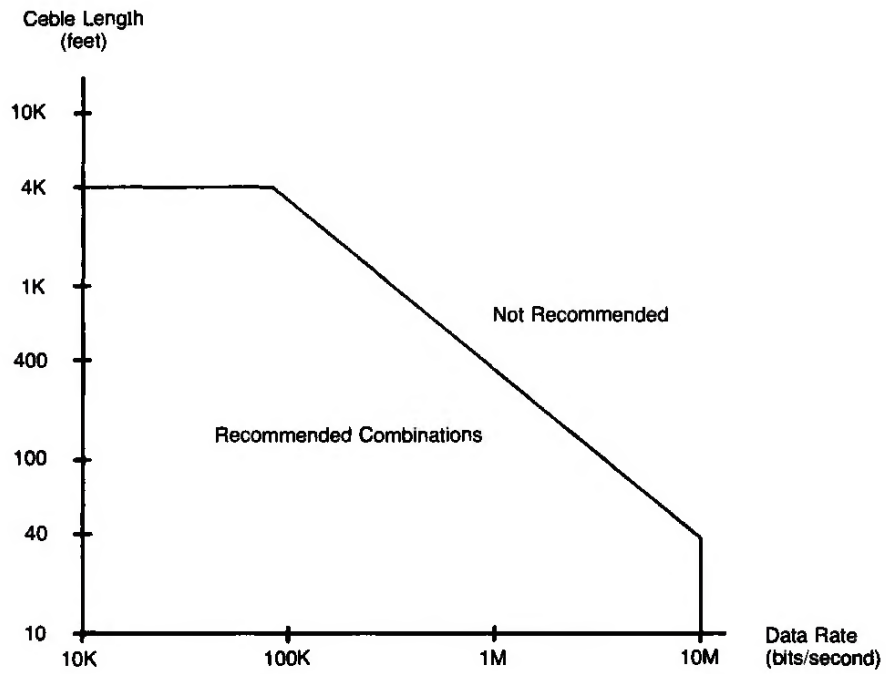
1 RS-422 cables for this interface are not available from Hewlett-Packard Company

RS-232C Data Rates

Up to 19,200 baud

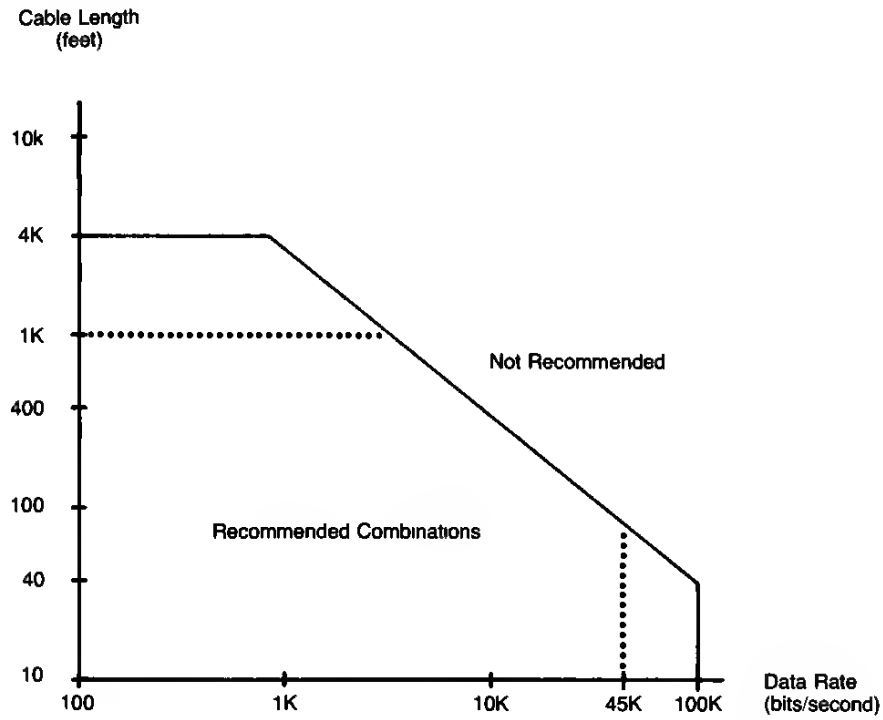
RS-449 Data Rates

Data rate limitations for RS-449 applications are dependent on cable length, but generally exceed the maximum rates available to RS-232C installations. The following charts show the maximum speed versus cable length for RS-422 (balanced) and RS-423 (unbalanced) RS-449 installations:



RS-422 Modulation Rate Versus Cable Length

The waveshaping used on the datacomm interface force a reduction in the maximum data rates that can be used for unbalanced transmissions. These limits are allowed by the RS-423 standard, and are indicated by the dotted lines in the following chart:



RS-423 Modulation Rate Versus Cable Length

RS-423 cables are discussed in Chapter 3.

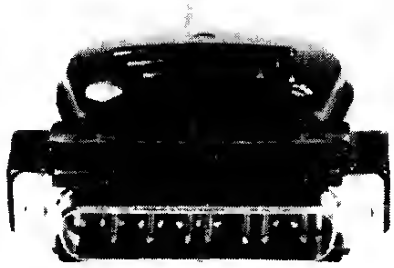
Cable Options

The HP 98628 and 98691 interfaces are available with 3 cable options which can also be ordered separately. Cable length is approximately 4.9 metres (16 feet). Cables are discussed in detail in Chapter 3.

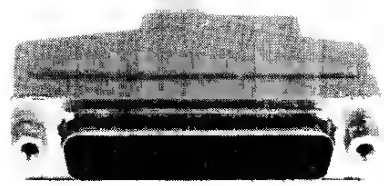
Option 001: RS-232C DTE Cable with 25-pin Male Connector
Used to connect to RS-232C DCE devices such as modems. Also available separately as part number 5061-4215.

Option 002: RS-232C DCE Cable with 25-pin Female Connector
Used to connect to male RS-232C DTE device cables. Connects to 5061-4215 or other terminal cables. Available separately as part number 5061-4216.

Option 003: RS-423 DTE Cable with 37-pin Male Connector
Unbalanced connections to RS-449/423 modems or other DCE devices. Available separately as part number 5061-4250.



Option 001 Male Connector



Option 002 Female Connector

Specialized Adapters

Three specialized adapters are available for use with the 98628A. They provide a means for connecting the 98628A to various data communications devices or links, and include the following:

- HP 13264A Data Link Adapter
- HP 13265A Modem
- HP 13266A Current Loop Adapter

Here is a brief description of each adapter:

The HP 13264A Data Link Adapter converts RS-232C signals from the 98628A to the differential signal levels required for HP DSN/Data Link connections.

The HP 13265A Modem is a Bell 103/113-compatible asynchronous modem for connecting directly to the US switched (public) telephone network. This modem is originate only, and is used in applications requiring up to 300 baud communications rates. It supports both auto dial and manual originate capability.

The HP 13266A Current Loop Adapter provides a 20 mA current loop interface for the 98628A. Current loop is used in applications that require data communications over longer distances than are possible with standard RS-232C. It is also used in electically noisy environments. The Current Loop Adapter can be configured with active or passive driver and receiver elements.

Chapter 2
Interface Configuration

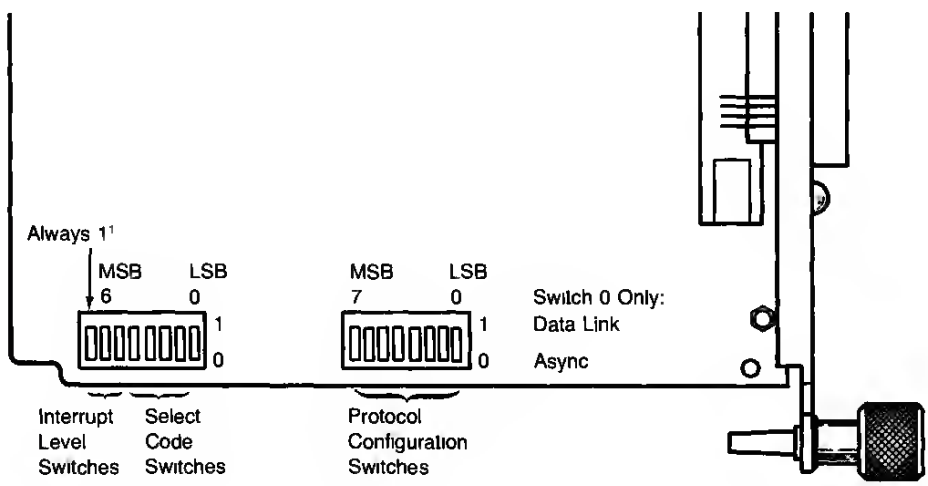
The datacomm interface is configured by use of two switch clusters located along one side of the interface card. These switches must be set to their proper positions before the interface is installed in the computer. This chapter discusses how to configure the interface for the various available options.

This chapter explains how to configure the HP 98628A Option 100 (Async/Data Link protocol) Datacomm Interface. If you are installing an HP 98691A Programmable Datacomm Interface (interface firmware designed by a supplier other than Hewlett-Packard Company), configure the select code and hardware interrupt level as described in this chapter, then configure the protocol switches using instructions provided by the supplier of the firmware that is installed on the interface card.

Configuration Switches

As shown in the following figure, the left-hand switch cluster is used to set the hardware interrupt level and interface select code. The left-most switch in that cluster has a function that is dependent on protocol and defined by interface firmware.

The function of the switches in the right-hand cluster is determined by protocol and the interface program ROM. These switches are discussed later in this chapter. The following figure shows the location of the configuration switches.



Interface Configuration Switches

1 This switch should always be set to 1 position on HP 98628 Datacomm Interface If you are using an HP 98691 Programmable Datacomm Interface, refer to firmware documentation supplied with the interface for the proper switch setting

When setting the configuration switches, be sure the switch rockers are fully depressed and properly seated. Switch settings can be changed by using a ball-point pen or a similar pointed tool to depress each switch rocker.

Interrupt Level and Select Code

This section discusses the switch settings of the left-hand cluster. The function of each of these switches, except one, is determined by interface hardware, and is not protocol dependent.

Remote Switch

The function of the left-most switch (switch 7) is protocol-dependent. If your interface is an HP 98628 (Async/Data Link Protocol), it is reserved for possible future use, and should be in the OFF (1) position. This ensures proper operation of the card during power-up and self-test operations. For the HP 98691 Programmable Datacomm Interface, consult the operating manuals provided by supplier of the special firmware installed on your interface.

Interrupt Level

The next two switches define the hardware interrupt level. Levels 1 and 2 are reserved for internal peripherals only, leaving interrupt levels 3 thru 6 available for interfaces to external peripherals. Interrupt level 3 is lowest priority; 6 is highest. If an interrupt request conflict occurs, service is provided by the computer on the basis of highest priority first. If two devices at the same level interrupt simultaneously, the interrupts are serviced in the order they are encountered by the operating system.

When assigning interrupt levels, don't forget that some interfaces may require that no other interface be placed at the same interrupt level (such as the HP 98625 High-speed Disc Interface used in Shared Resource Management applications). The factory-default setting of interrupt level 3 is adequate for most applications. Here is a listing of the available interrupt level settings:

Interrupt Level Switch Settings

Switch Settings 6	5	Interrupt Level
0	0	3
0	1	4
1	0	5
1	1	6

Interface Select Code

Each internal peripheral and external peripheral interface has a unique interface select code by which it is accessed when the operating system must transfer information to or from that device. The interface select code is determined by hardware settings, but the interaction can vary, depending on the operating system and software being used.

Select codes 1 thru 6 are reserved for internal peripherals such as the keyboard, disc drives, CRT display and other devices. Select code 7 is used by the internal HP-IB interface, leaving select codes 8 thru 31 available for other interfaces to external peripherals. However, not all language options support the entire range of select codes, and default select codes for certain devices may vary, depending on the language being used. Refer to the interfacing or I/O manual for the language being used for more information about restrictions on select code values.

Some general guidelines apply to select code assignment regardless of which language is being used. The most important restriction is that you must never set more than one interface to a given select code value. Otherwise, the interfaces compete whenever any information transfer or control or status operation is performed on that select code. Each interface is marked with a recommended default setting. This setting is adequate for most languages, but may have to be altered in some specific instances, especially if one computer is being used for multi-language applications, and supports several peripherals.

Note

When assigning a select code other than the one printed on the interface cover, check the select code assignments for all other interface cards in the system. Do not assign the same select code to more than one interface.

Here are the available interface select code switch settings. The default setting of 20 is highlighted.

Select Code Settings

Select Code	MSB 43210 LSB	Select Code	MSB 43210 LSB
0 thru 7	Do not use	**20**	**10100**
8	01000	21	10101
9	01001	22	10110
10	01010	23	10111
11	01011	24	11000
12	01100	25	11001
13	01101	26	11010
14	01110	27	11011
15	01111	28	11100
16	01100	29	11101
17	10001	30	11110
18	10010	31	11111
19	10011		

Protocol Configuration

During system power-up or reset, the right-hand switch cluster configures protocol-dependent default operating parameters or functions. On the HP 98628 (Async/Data Link protocol) interface, these switches establish various operating parameters such as handshake protocol and baud rate. For the HP 98691, refer to the applicable firmware and protocol operating manuals for the needed information.

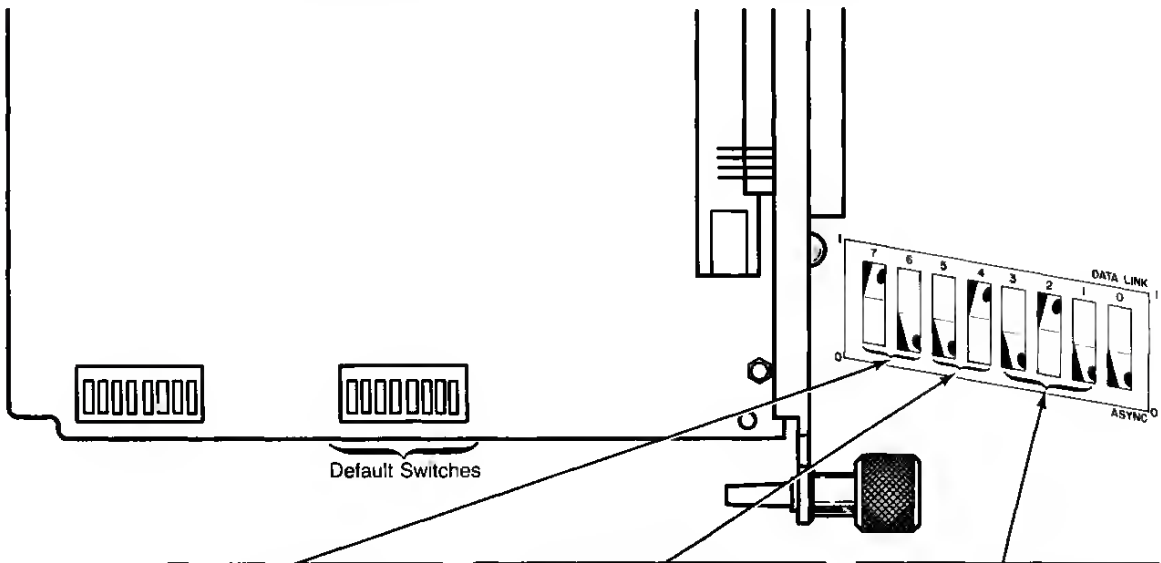
This section discusses protocol configuration switch settings for the Async/Data Link protocol interface, 98628A Option 100.

Async/Data Link Protocol Selection

The right-most (bit 0) switch in the default cluster selects the power-up default of asynchronous (Async) or DSN/DL (Data Link) protocol. The function of the remaining 7 switches depends on which protocol is selected.

Async Protocol Default Configuration

At power-up, the datacomm interface is automatically configured using the default switch settings. The initial configuration can be altered under program control by the use of CONTROL and STATUS statements in BASIC, or their equivalent in other languages. To use the default values, omit the corresponding control operations from your program. When Async protocol is selected[1], the remaining 7 switches have the following functions:



Parity	Bits/Char
00 = None	8
01 = None	7
10 = Odd	**7**
11 = Even	7

Hardware Handshake
00 = Handshake OFF, non-modem connection[1]
01 = FULL Duplex modem connection[2]
10 = HALF Duplex modem connection[2]
11 = Handshake ON, non-modem connection[1]

Baud Rate	Stop Bits
000 = 110	2
001 = 150	2
010 = 300	**1**
011 = 600	1
100 = 1200	1
101 = 2400	1
110 = 4800	1
111 = 9600	1

Async Default Configuration Switches

1 Protocol can also be overridden by CONTROL operations, but the other parameters established by default switches must be replaced by CONTROL operations in order to ensure proper configuration

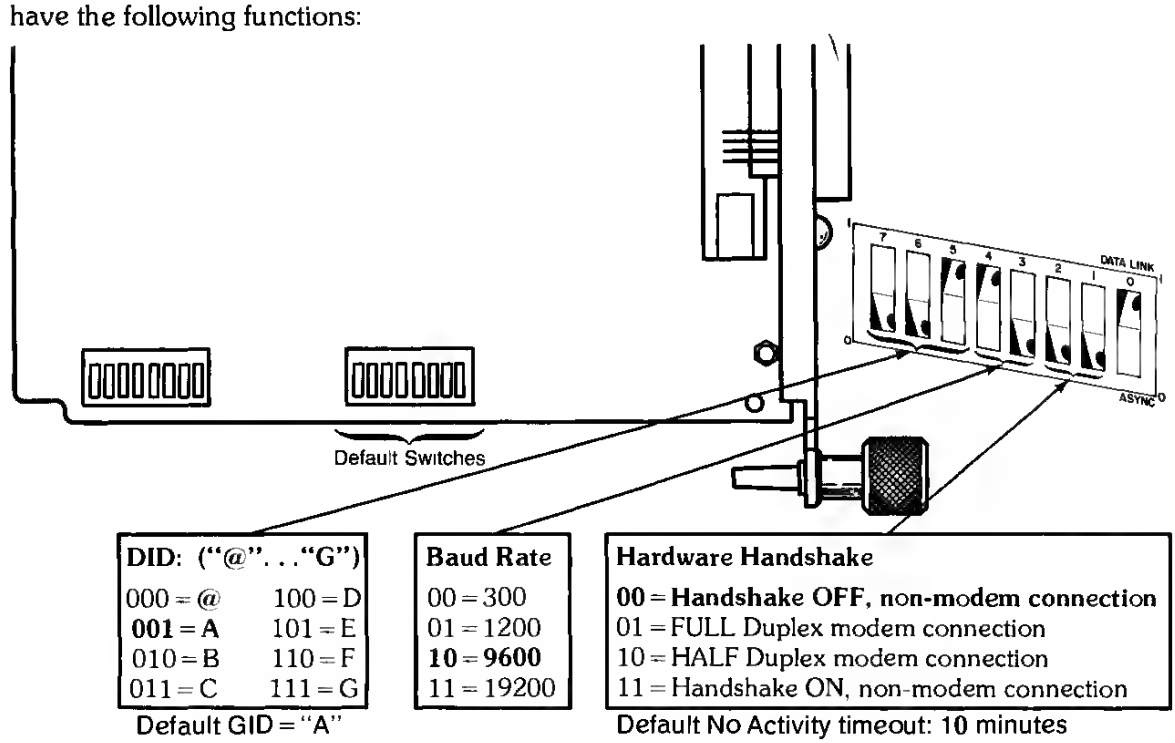
Before you set up the default switches, determine the proper operating parameters for your application, then set the parity, hardware handshake, and baud rate switches as indicated in the figure. Be sure that all switches are fully seated in their proper positions to ensure proper operation.

Character format parameters are determined by the requirements of the device at the other end of the datacomm link. If default switches are used to establish operating parameters, only parity and baud rate can be selected. Bits per character and stop bits per character are determined by the parity and baud rate settings. Default switch settings can be overridden under program control. Control register operations can be used to independently program all character format parameters (for example, bits per character and stop bits are not dependent on baud rate or parity settings). Status register operations can be used to determine current interface settings. Values returned represent current operation, and may not match the current default switch settings if a previous Control operation has overridden the switches.

For 3-wire non-modem connections, the hardware handshake is set to handshake OFF, non-modem connection. If the full complement of handshake signals such as data terminal ready, clear-to-send, etc. are available in non-modem connections, then set the switches to hardware handshake ON, non-modem connection. If modems are being used, set half/full duplex to the appropriate configuration. This completes default switch configuration for Async connections.

Data Link Protocol Default Configuration

As when Async protocol is selected, the datacomm interface is automatically configured at power-up according to default switch settings. The initial configuration can be altered under program control by the use of CONTROL and STATUS statements in BASIC, or their equivalent in other languages. To use the default switch settings, omit the corresponding control operations from your program. When Data Link protocol is selected[1], the remaining 7 switches have the following functions:


DATA LINK
ASYNC
Default Switches
DID: ("@"..."G")
000 = @ 100 = D
001 = A 101 = E
010 = B 110 = F
011 = C 111 = G
Default GID = "A"
Baud Rate
00 = 300
01 = 1200
10 = 9600
11 = 19200
Hardware Handshake
00 = Handshake OFF, non-modem connection
01 = FULL Duplex modem connection
10 = HALF Duplex modem connection
11 = Handshake ON, non-modem connection
Default No Activity timeout: 10 minutes

Data Link Default Configuration Switches

1 Protocol can also be overridden by CONTROL operations, but the other parameters established by default switches must be replaced by CONTROL operations in order to ensure proper configuration.

Before you set up the default switches, determine the proper operating parameters for your application, then set the parity, hardware handshake, and baud rate switches as indicated in the figure. Be sure that all switches are fully seated in their proper positions to ensure reliable operation.

Interface Installation

After the configuration switches have been set, you are ready to install the interface in the computer. Most computers that use this interface have one or more I/O backplane cover plates that protect the accessory/backplane enclosure. To install the interface, remove the appropriate cover and carefully slide the interface into the selected slot, usually the one below the centerline of the cover plate retainer nuts in the computer or expander frame. Seat the interface into the backplane connector, then tighten the two thumbscrews to hold the interface in place. Do not overtighten. The interface is now ready to be connected to an interconnecting cable or adapter between the interface and whatever data communication equipment you are using in your application.

Chapter 3
Interface Cables

Before the datacomm interface can interact with a remote computer or other device, it must be connected to the data communications link. This can be a simple direct connection to a host computer nearby, or it can be to a modem or other device that uses a more sophisticated connection such as a switched telephone network connection or satellite microwave link. The type of connection determines what type of cable is needed for a given application. This chapter explains how to connect cables for various applications, and includes schematic diagrams of the cable options available for the datacomm interface.

RS-232C Connections

There are two types of cables available for RS-232C applications. Both are equipped with 25-pin EIA connectors designed to mate with connectors on other RS-232C devices or equipment.

- The Option 001 (DTE) cable has a male connector, and is designed for connecting the interface to an RS-232C-compatible modem or other data communications equipment. The DTE designation means the cable is designed to be used as a Data Terminal Equipment (DTE) interconnect to Data Communications Equipment (DCE).
- The Option 002 (DCE) cable has a female connector and is internally cross-wired so that the datacomm interface acts like DCE, such as a modem. Thus, by using two cables, one of each type, two computers can be connected directly to each other, back-to-back, without using modems or other devices between the two.

Optional Drivers and Receivers

Two optional drivers and receivers are used with the RS-232C cable options[1]. Their functions are as follows.

Drivers	
Name	**Function**
OCD1	Data Rate Select
OCD2	Secondary Request to Send
OCD3	Not used
OCD4	Not used

Receivers	
Name	**Function**
OCR1	Ring Indicator
OCR2	Secondary Data Carrier Detect

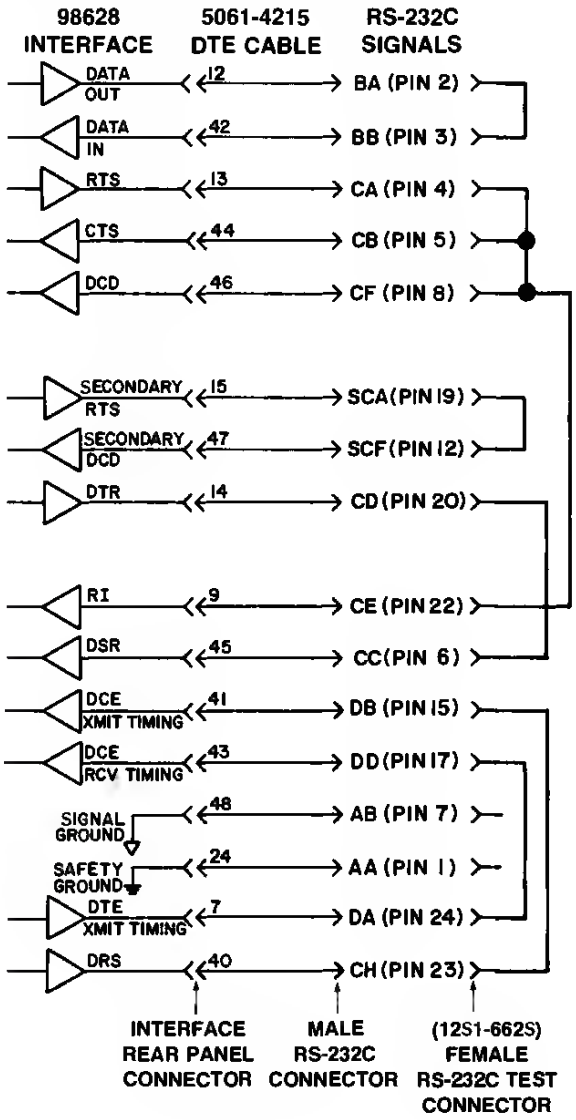
OCD2 is used for auto-dial pulsing in the HP 13265A Modem. None of the optional drivers and receivers are used for Data Link and Current Loop adapters.

1 These driver and receiver assignments are for the HP 98628 Datacomm Interface, and may not apply to the HP 98691 Programmable Datacomm Interface. Refer to documentation from the firmware supplier for that information.

Option 001 DTE (Male) Cable

The male DTE cable (5061-4215) is compatible with most RS-232C modems. It is designed so that you can connect a modem directly to the datacomm interface without using an intermediate adapter.

The following cable schematic shows which drivers and receivers are connected to respective pins in the male RS-232C connector. It also includes the test connector schematic showing the loop-back signal paths used for testing the interface and cable.

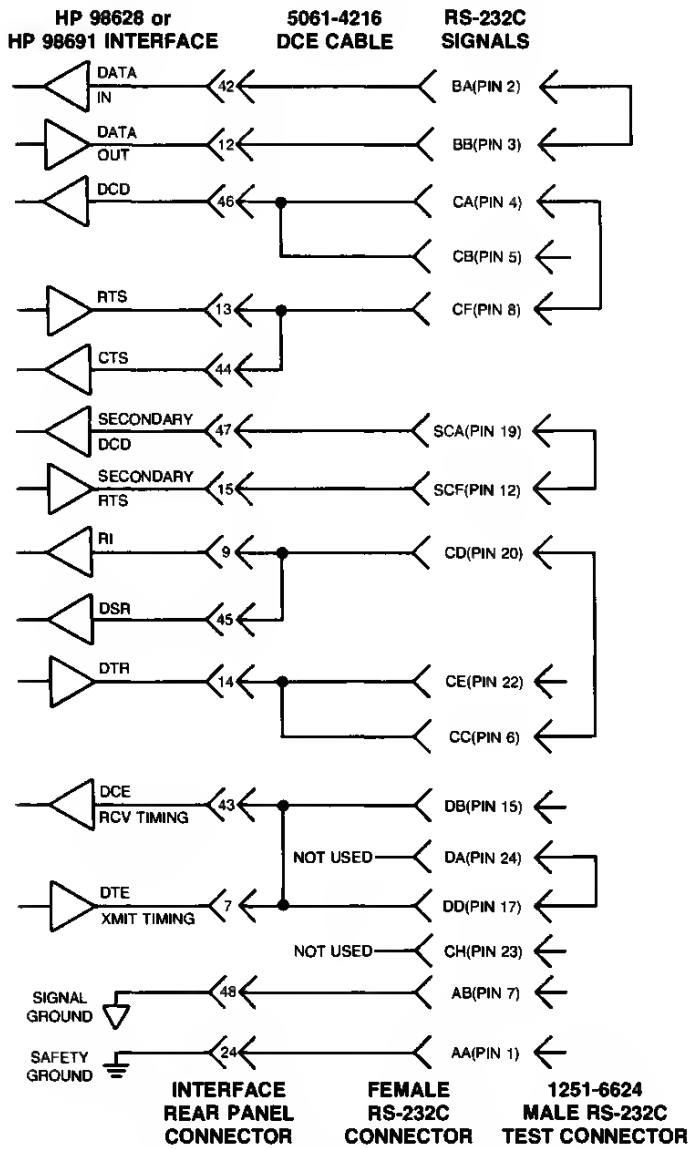


Option 001 DTE Interface Cable and Test Connector

Option 002 DCE (Female) Cable

The female DCE cable (5061-4216) is compatible with the Option 001 male DTE cable for all back-to-back connections between desktop computers equipped with HP 98628A datacomm interfaces. The DCE cable can also be used successfully with most male DTE RS-232C cable connectors designed for driving modems.

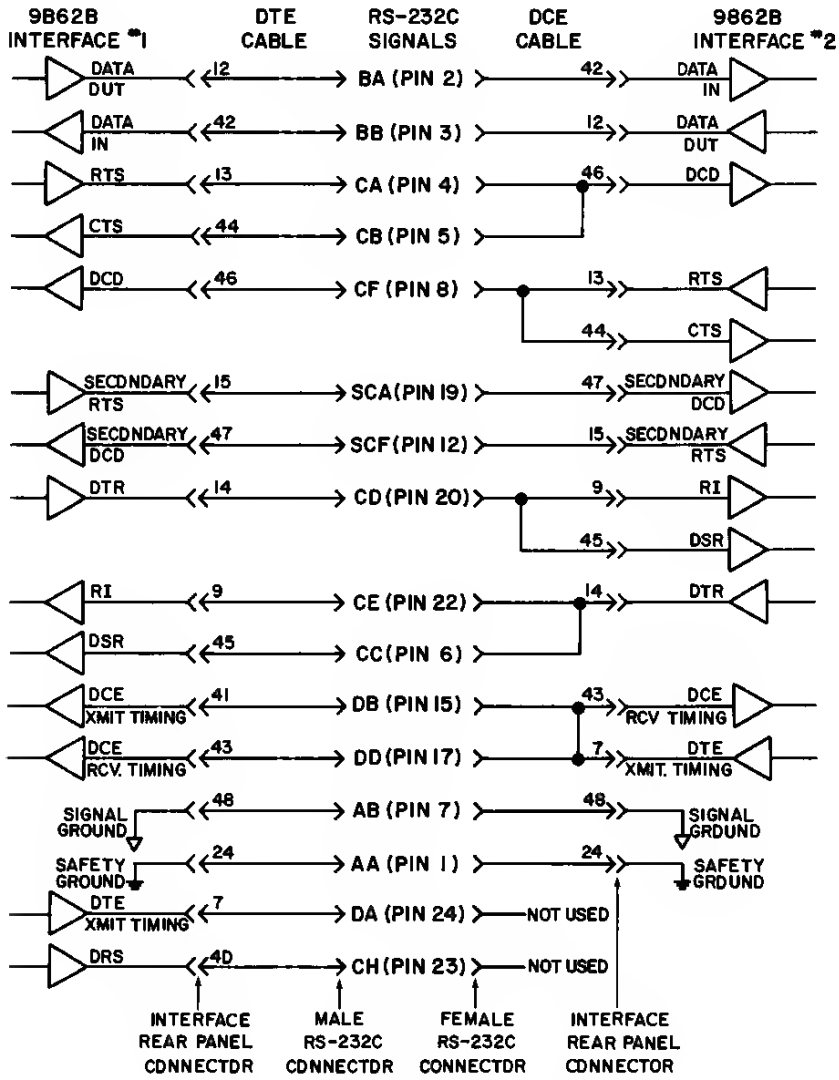
The following diagram shows the driver and receiver connections to the female RS-232C connector, and includes the test connector loop-back wiring:



Option 002 DCE Interface Cable and Test Connector

Connecting Two Desktop Computers

The HP 98628 Datacomm Interface can be used in a back-to-back configuration to connect two desktop computers to each other. To ensure proper signal flow, connect the two datacomm interfaces to each other by using an Option 001 (DTE) cable on either interface, and an Option 002 (DCE) cable on the other. The DCE cable includes some internal cross-wiring to connect interface signals so that they simulate normal modem (DCE) operation. The following schematic diagram shows the interconnection between interfaces through the two cables, and includes all connector pin numbers.



DTE/DCE Interface Cable Wiring

Using DCE Cables to Connect to DTE Devices

Sometimes, you may want to connect the datacomm interface to an RS-232C printer or other peripheral that has a female DTE connector on its rear panel. The obvious question then is which cable option should you use? In truth, neither will work, because:

- The DCE cable that would normally be used to interconnect to DTE devices has a female connector, thus requiring an adapter, and
- The male DTE cable is not pin-compatible because each signal line connects two drivers or two receivers, causing conflicts between drivers and no signal source for the receivers.

To connect the datacomm interface to an RS-232C peripheral, use an adapter cable that is suited to your needs. Several stock cables are available from HP, or you can wire your own, depending on the situation. Factors that affect cable selection include:

- Does the peripheral provide all the required handshake inputs for the interface?
- Does the peripheral have receivers that can produce the needed response to the driver signals originating from the interface?
- What signals must be cross-wired to maintain the proper states for the various handshake lines such as DSR, CTS, and RI?

For more information about what stock adapter cables are available for your needs, contact your nearest HP Sales and Service office.

RS-449 Connections

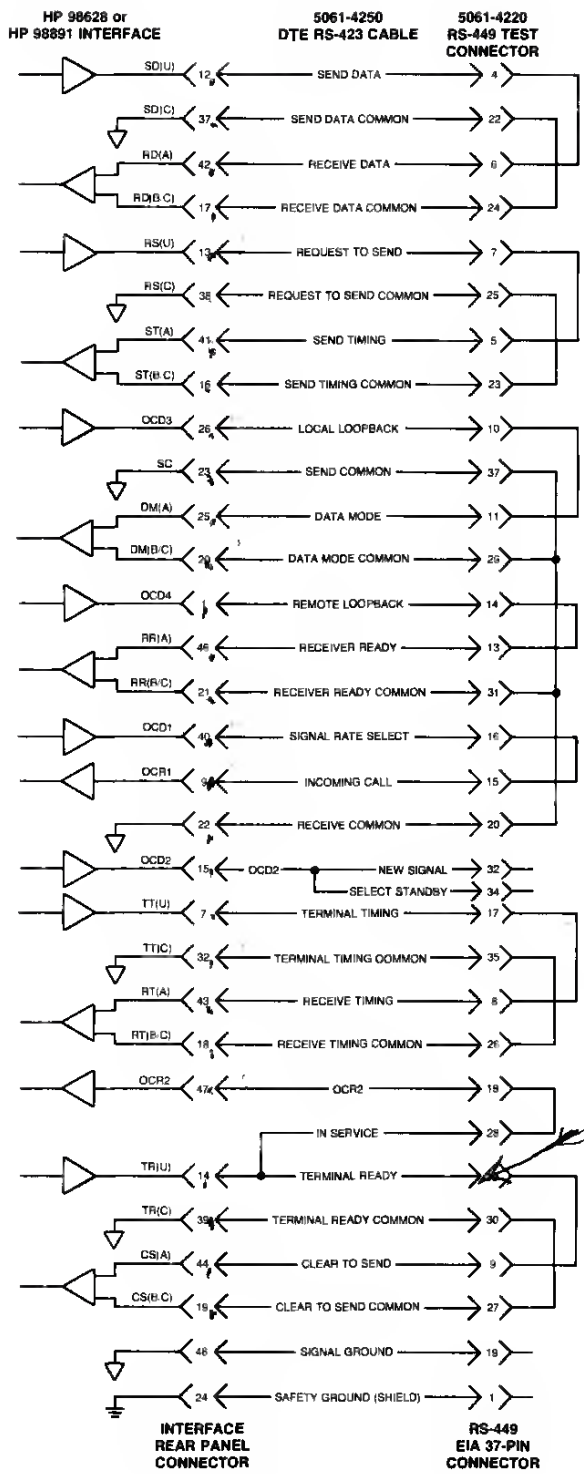
There are two types of RS-449 Interface configurations:

- RS-422 Balanced-line interconnection, and
- RS-423 Unbalanced-line interconnection.

Cable options for RS-449/422 are not available from HP at the present time.

Option 003 RS-423 Unbalanced DTE Cable

The HP 98628A Option 003 interface includes an interface cable (5061-4250) that is compatible with RS-449/423 unbalanced applications. The interface cable connector is a male DTE connector designed to mate with a female DCE connector. The following diagram shows the wiring configuration of the RS-423 cable and connectors including interconnection to drivers, receivers, and grounds, as well as test connector loop-back wiring.



RS-423 Unbalanced-line Interface Cable

Test Connectors

Test connectors are furnished with cable options to the datacomm interface. Interfaces shipped without cables do not include a test connector.

RS-232C DTE Cable Test Connector

A female 25-pin test connector (1251-6625) is shipped with the male DTE cable. The connector has several pairs of pins shorted to each other to provide signal loop-back. The following table shows how the connector is wired, and includes the identification of the signal lines that are tied together:

RS-232C DTE Test Connector Loop-back Wiring

Signal Source Name	RS-232C ID	Pin #	Pin #	RS-232C ID	Signal Destination Name
Transmit Data	BA	2	3	BB	Receive Data
Request to Send	CA	4	5,8,22	CB/CF/CE	Clear to Send/ Data Carrier Detect/ Ring Indicator (OCR1)
Data Terminal Ready	CD	20	6	CC	Data Set Ready
Secondary RTS	SCA	19	12	SCF	Secondary DCD (OCR2)
(not used)		14	25		(not used)
Data Rate Select (OCD1)	CH	23	15	DB	DCE Transmit Timing
Terminal Xmit Timing	DA	24	17	DD	DCE Receive Timing

RS-232C DCE Cable Test Connector

A test connector (1251-6624) is also provided with the datacomm interface DCE cable option. This connector is similar to the DTE test connector, except that it is male instead of female, and two jumpers have been omitted. The following table shows the loop-back wiring connections:

RS-232C DCE Cable Test Connector Loop-back Wiring

Signal Source Name	RS-232C ID	Pin #	Pin #	RS-232C ID	Signal Destination Name
Transmit Data	BA	2	3	BB	Receive Data
Request to Send	CA	4	8	CF	Data Carrier Detect
Data Terminal Ready	CD	20	6	CC	Data Set Ready
Secondary RTS	SCA	19	12	SCF	Secondary DCD (OCR2)
Terminal Xmit Timing	DA	24	17	DD	DCE Receive Timing

RS-449 Cable Test Connector

A female 37-pin test connector (5061-4220) is shipped with the RS-449/423 (Option 003) cable. Like its RS-232C counterparts, the connector has several pairs of pins shorted to each other to provide signal loop-back. The following table shows connector wiring and signal identification:

RS-449 Test Connector Loop-back Wiring

Signal Source Name	RS-232C ID	Pin #	Pin #	RS-232C ID	Signal Destination Name
Send Data (unbal)	SD(u)	4	6	RD(A)	Receive Data
Send Data Common	SD(C)	22	24	RD(B/C)	Receive Data Common
Request to Send (unbal)	RS(u)	7	5	ST(A)	Send Timing
Request To Send Common	RS(C)	25	23	ST(B/C)	Send Timing Common
Local Loopback	OCD3	10	11	DM(A)	Data Mode
Send Common	SC	37	29	DM(B/C)	Data Mode Common,
			20	RC	Receive Common,
			31	RR(B/C)	Receiver Ready Common
Remote Loopback	OCD4	14	13	RR(A)	Receiver Ready
Signal Rate Select	OCD1	16	15	OCR1	Incoming Call
Terminal Timing (unbal)	TT(u)	17	8	RT(A)	Receive Timing
Terminal Timing Common	TT(C)	35	26	RT(B/C)	Receive Timing Common
Terminal Ready (unbal)	TR(u)	12	9	CS(A)	Clear to Send
Terminal Ready Common	TR(C)	30	27	CS(B/C)	Clear to Send Common
Terminal Ready (unbal)	TR(u)	28	18	OCR2	Test Mode

Building Custom Cables

Occasional situations may require use of non-standard cables. If you need to modify an existing cable or design a new one, several precautions are necessary to ensure optimum performance. This section provides information for determining wiring needs and suggests several helpful assembly techniques that can produce better noise immunity and better system performance.

Safety Considerations

Electrical equipment safety grounds must be adequately maintained when designing cables. Generally, a shielded multi-conductor cable is used for datacomm applications. The outer shield is wired to the earth (safety) ground pin on the interface connector. The shield should also be continued with a connection through the cable terminating connector to the safety (earth or frame) ground of the device being connected. Grounding the shield at both ends provides a path for electrostatic discharge currents, and helps maintain both frames at the same potential, thus improving noise immunity. Be sure, however, that there are no ground voltage differentials between power receptacles for devices connected to the same cable shield. This is best ensured by feeding power to both the computer and modem or other device from the same circuit breaker panel, or by taking other equivalent precautions.

For other than short cable runs, to ensure safe ground currents through the shield, install the cable so that it is connected to the datacomm interface after the interface is installed in the computer and the computer power has been connected. If the modem and computer are connected to a different building grounds: before you connect the cable to the modem, use an AC/DC digital voltmeter to measure the voltage difference between the shield pin of the cable connector and the shield pin of the corresponding modem (or other device) connector. If the voltage is more than 100 to 300 millivolts, alternate grounding should be installed to reduce or eliminate the difference. After grounding is complete and cables are connected, use a current-sense probe to measure cable shield currents. Shield currents at power frequency or below should never be allowed to exceed a few hundred milliamperes under normal operating conditions.

Using Interface Power Connections

The datacomm interface provides pins for +5V, +12V, and −12V power at its rear panel connector. These connections are normally used with various modems or adapters supplied by HP, and are not intended for other purposes. Improper use of these power connections can seriously compromise the reliability of the computer.

Balanced Versus Unbalanced Connections

Note that the interface is designed for both balanced (RS-449/422) and unbalanced (RS-449/423 and RS-232C) operation. This requires a dual set of drivers for certain outputs as well as receivers that support both balanced and unbalanced inputs. All connections to the interface cable or adapter are made through the 50-pin connector on the interface rear panel cover. Connections are shown on the schematic diagram, and a suffix on each line identifier indicates whether the input or output is for balanced or unbalanced operation as follows:

- TT(u), SD(u), TR(u), and RS(u) are all unbalanced driver outputs whose return paths to ground are to TT(C), SD(C), TR(C) and RS(C), respectively.
- Balanced drivers for TT, SD, TR, and RS have their complementary outputs labelled as: (A) for inverted output; (B) for non-inverted output.

- Receiver inputs ST, RT, RD, and CS that are labelled (A) are connected to the (A) output of the associated balanced driver or the output from the unbalanced driver for that line. The (B/C) input is connected to the balanced driver (B) output, or to the (C) return ground path for unbalanced drivers. Be careful to maintain proper signal sense through the interface cables to ensure correct logic sense in received data bits.
- All other drivers and receivers are unbalanced lines with ground returns handled through the SC (signal common) and SG (signal ground) lines. The cable shield should not be connected to the same connector pin(s) as the common/ground signal return lines.
- Balanced-line interface cables used in RS-422 applications must be properly terminated to minimize or eliminate transmission-line reflections due to impedance mismatch. This is usually accomplished by adding a load resistor (approximately 100Ω) across each balanced receiver input. The impedance of the receiver input(s) and associated circuitry should be considered when determining the proper load resistance to be used.

The following table shows datacomm rear panel pinouts for both balanced and unbalanced RS-232C and RS-449 applications.

Datacomm Interface Connector Pin Assignments

Function	Interface Pin No	Interface Pin No	Function
Optional Driver OCD4	1	26	Optional Driver OCD3
Send Data (SD) bal (B)	2	27	Send Data (SD) bal (A)
Req to Send (RS) bal (B)	3	28	Req to Send (RS) bal (A)
Terminal Ready (TR) bal (B)	4	29	Terminal Ready (TR) bal (A)
Not used	5	30	Not used
Not used	6	31	Not used
Xmit Timing (TT) unbal	7	32	Xmit Timing (TT) unbal return
Xmit Timing (TT) bal (B)	8	33	Xmit Timing (TT) bal (A)
Ring Indicator (OCR1)	9	34	
Modem/Adapter Power: +12V	10	35	Modem/Adapter Power: +5V
Modem/Adapter Power: −12V	11	36	Connected to pin 35
Send Data (SD) unbal	12	37	Send Data (SD) unbal return
Request to Send (RS) unbal	13	38	Req to Send (RS) unbal return
Terminal Ready (TR) unbal	14	39	Term Ready (TR) unbal return
Secondary RS (OCD2)	15	40	Data Rate Select (OCD1)
Send Timing (ST) input (B/C)	16	41	Send Timing (ST) input (A)
Receive Data (RD) input (B/C)	17	42	Receive Data (RD) input (A)
Rcv Timing (RT) input (B/C)	18	43	Receive Timing (RT) input (A)
Clear to Send (CS) input (B/C)	19	44	Clear to Send (CS) input (A)
DM (RS-449)/DSR (RS-232) (B/C)	20	45	RS-232C Data Set Ready
Rcvr Ready (Data Carrier Detect) RR input (B/C)	21	46	Rcvr Ready (Data Carrier Detect) RR input (A)
Receive Common (RC)	22	47	Secondary DCD (OCR2)
Send Common (SC)	23	48	Signal Ground
Earth (Safety) Ground (Shield)	24	49	Not used
Data Mode (DM) input (A) RS-449	25	50	Not used

Unbalanced returns for TT (pin 32), SD, RS, and TR (pins 37, 38, and 39) are connected to logic ground, as are SC (pin 23) and SG (pin 48).

Power supplied from pins 10, 11, 35, and 36 is normally used for modems and adapters supplied by HP, and is not intended for other purposes. Improper use of these pins can seriously compromise the reliability of the computer that powers the interface.

Comparison of Datacomm Standards

There are three dominant datacomm standards, RS-232, RS-449, and CCITT V.24 which is used mainly in Europe. Each uses mnemonics or numbers to identify various signal lines and grounds. The following table is provided for your convenience in interpreting standards and relating them to the datacomm interface. Not all functions are supported by the interface.

Electrical Standards Comparison Table

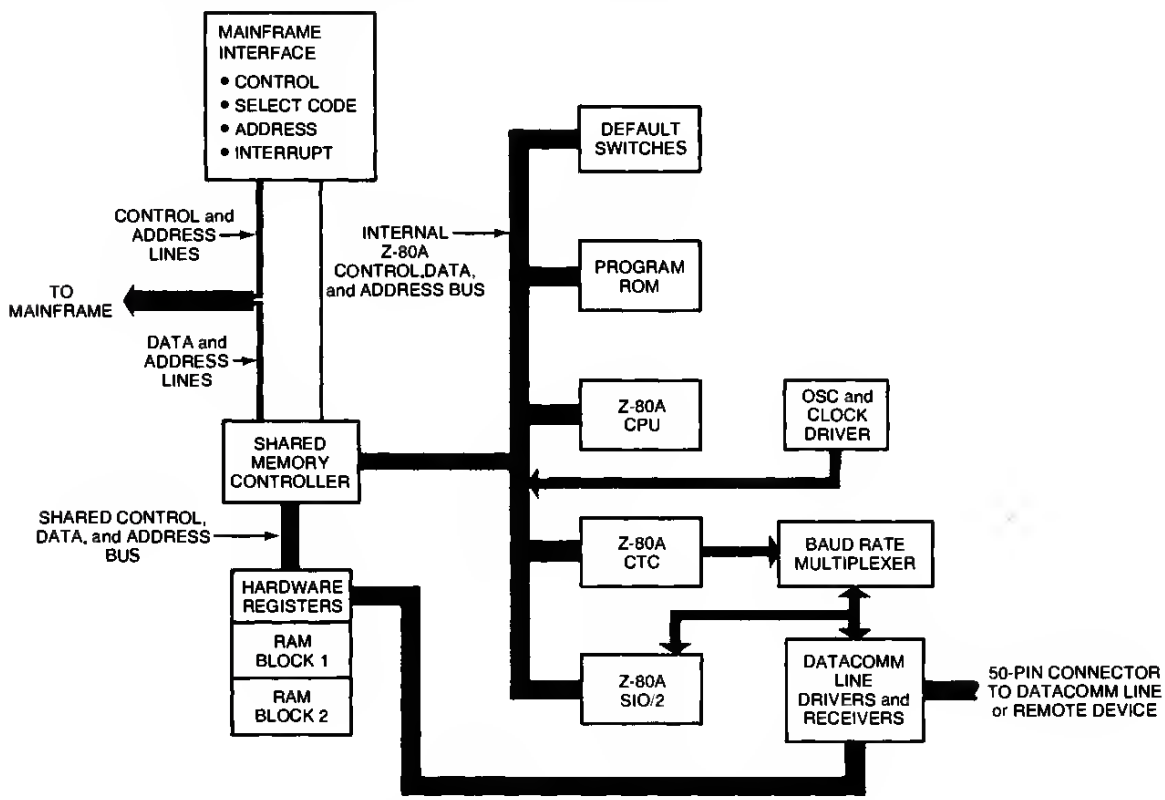
	RS-449		**RS-232C**		CCITT V.24
SG	Signal Ground	AB	Signal Ground	102	Signal Ground
SC	Send Common		(not assigned)	102a	DTE Common
RC	Receive Common		(not assigned)	102b	DCE Common
IS	Term. in Service		(not assigned)		(not assigned)
IC	Incoming Call	CE	Ring Indicator	125	Calling Indicator
TR	Terminal Ready	CD	Data Terminal Ready	108/2	Data Terminal Ready
DM	Data Mode	CC	Data Set Ready	107	Data Set Ready
SD	Send Data	BA	Transmitted Data	103	Transmitted Data
RD	Receive Data	BB	Received Data		Received Data
TT	Terminal Timing	DA	Tx Timing (DTE)	113	Tx Timing (DTE)
ST	Send Timing	DB	Tx Timing (DCE)	114	Tx Timing (DCE)
RT	Receive Timing	DD	Receiver Timing	115	Rec Timing (DCE)
RS	Request to Send	CA	Request to Send	105	Request to Send
CS	Clear to Send	CB	Clear to Send	108	Ready for Sending
RR	Receiver Ready	CF	Data Carrier Detect	109	Received Line Signal Detect
SQ	Signal Quality	CG	Signal Quality Detector	110	Data Signal Quality Detector
NS	New Signal		(not assigned)		(not assigned)
SF	Select Frequency		(not assigned)	126	Select Tx Frequency
SR	Signalling Rate Selector	CH	Data Signal Rate Selector (DTE)	111	Data Signalling Rate Selector (DTE)
SI	Signal Rate Indicator	CI	Data Signal Rate Selector (DCE)	112	Data Signalling Rate Selector (DCE)
SSD	Secondary Send Data	SBA	Secondary Transmitted Data	118	Transmitted Backward Channel Data
SRD	Secondary Receive Data	SBB	Secondary Received Data	119	Received Backward Channel Data
SRS	Secondary Request to Send	SCA	Secondary Request to Send	120	Transmit Back Channel Line Signal
SCS	Secondary Clear to Send	SCB	Secondary Clear to Send	121	Backward Channel Ready
SRR	Secondary Receiver Ready	SCF	Secondary Data Carrier Detect	122	Backward Channel Receiver Line Signal Detect
LL	Local Loopback		(not assigned)	141	Local Loopback
RL	Remote Loopback		(not assigned)	140	Remote Loopback
TM	Test Mode		(not assigned)	142	Test Indicator
SS	Select Standby		(not assigned)	116	Select Standby
SB	Standby Indicator		(not assigned)	117	Standby Indicator

Chapter 4
Service Information

This chapter contains a summary of interface theory of operation and other information needed to service the datacomm interface at component level. Troubleshooting and repair should be done by expert technicians who are familiar with Z-80A microprocessor circuit operation, and who have access to Z-80A documentation when needed. Detailed interface theory is not provided. This interface is normally serviced on an exchange/replacement basis due to its complexity. Service at the component level should be attempted only when adequate test equipment is available.

Theory of Operation

The following block diagram shows the functional blocks that comprise the interface.



Datacomm Interface Block Diagram

The interface communicates with the computer mainframe through interface circuitry that is treated like memory addresses by the mainframe. Information is exchanged between the interface and computer through shared RAM memory and hardware registers. Access to shared memory and hardware registers is obtained through the shared memory controller. Data is transferred on the shared data bus. Interaction between the interface and computer mainframe is managed by interrupt circuitry and the address comparator connected to the upper bits of the mainframe memory address bus.

The interface program ROM usually contains operating firmware for the Z-80A interface CPU which executes the protocol-dependent programs stored in the ROM. Shared memory is used to exchange information between the interface CPU and the mainframe computer. The interface CPU controls the SIO and CTC chips which perform datacomm serial I/O operations (SIO) and counter and timing functions (CTC). It also performs and controls various other interface functions on command from the mainframe processor.

The modem control register latch and modem status register buffer hold control and status information being exchanged between the modem and interface. Line drivers and receivers convert the internal TTL signals to RS-232C or RS-449 electrical levels for transmission over the datacomm link. Data format and protocol information are created by the interface CPU with help from the CTC and SIO support chips. Default switch information is used by the interface CPU to set up power-up and reset defaults as defined by the firmware in the Program ROM.

Z-80A System Operation

The Z-80A CPU, SIO, and CTC chips as well as the program ROM and default switches are tied together through the internal Z-80A 16-bit address (ZA) bus and 8-bit data (ZD) bus. These buses belong exclusively to the interface CPU and are not accessible by the mainframe computer.

Shared RAM and registers are accessed through the shared data (SD) and shared address (SA) buses. Access to the shared buses is controlled by the shared memory controller. In general, bus access is granted to the first processor that requests the bus. If the shared memory controller grants access to one processor and the other processor requests access during the memory cycle, the controller holds the second processor off until the memory cycle is complete, after which shared memory access is granted to the second processor. If a simultaneous-request conflict occurs, bus access defaults to the mainframe. Only 15 bits of address bus and 8 bits of data bus are gated to the shared buses from the mainframe. The remaining mainframe address bus bits are gated to the address comparator to establish select code identification. The address comparator bits combine with the shared address bus bits to establish the range of mainframe memory addresses that pertain to a particular interface. Upper-byte mainframe data bus bits (8 thru 15) are not used by the interface.

Select Code Recognition

The Address Decoder (U43) decodes mainframe upper memory address bits to detect card accesses. The BAS input from the mainframe gates the comparator inputs to ensure that the address is stable. When the address is recognized, the P = Q output is activated causing the IMA (I'm Addressed) output to return acknowledgement to the mainframe. The DTACK (Data Acknowledge) output is also enabled, and is activated later by the Shared Memory Controller.

BLDS (Buffered Lower Data Strobe, and MYPA (My Peripheral Address) are ANDed with the Request Enable flip-flop (U23 Pin 4) to produce the mainframe shared memory request signal, one of the inputs to the Shared Memory Controller. The Request Enable flip-flop ensures that the Shared Memory Controller has completed any memory cycles in process before granting access for a new one, since the mainframe and interface processors are not synchronized with each other.

Interrupt System

The mainframe driver enables or disables interface interrupts by sending control sequences to the shared data bus that set or clear the Interrupt Enable flip-flop (U14 pin 5) through a hardware register access.

When the interface card determines that service from the mainframe is required, the interrupt condition is sent to a register in shared memory. The memory write cycle automatically resets the Interrupt Request flip-flop (U23 pins 9 and 10: pin 9 goes low on reset). If interrupts are enabled (Interrupt Enable Q output is low), and service is requested (Interrupt Request Q output is low), the Interrupt Demultiplexer (U34) is enabled. When the enable signal is received by the Interrupt Demultiplexer, the interrupt level switches are decoded (SW2 pins 6 and 7), which activates one of the interrupt request lines (IR3 thru IR6).

Interrupt requests are cleared by the mainframe when it reads the Interrupt Cause register in shared memory. The interrupt request is removed when the Interrupt Register Decoder (U22) activates one of the Set inputs on the Interrupt Request flip-flop.

Interface Reset

During power-up, the computer mainframe pulls the RESET input on all interface cards low. This causes the datacomm interface to reset the Z-80A CPU by activating its reset input for the duration of the pulse, and clears the Reset flip-flop (U15 pin 9). When the Reset flip-flop Q output goes low, it resets or presets other flip-flops that must be initialized to a known state. The Z-80A CPU then disables the Reset flip-flop during execution of its reset routines. A shared hardware register access is used to terminate the hardware reset.

When a control register operation is used to reset the card, the control sequence is handled through the shared memory controller which sends the reset command to the Reset flip-flop. The flip-flop then:

- Disables mainframe interrupts by setting the Interrupt Enable flip-flop.
- Disables mainframe interrupt requests by setting the Interrupt Request flip-flop.
- Clears the hardware Semaphore flip-flop (semaphore busy).
- Initializes the CTC and SIO Z-80A support chips by activating their Reset inputs.
- Disables Modem Control Latch (U3) outputs to ensure that the Terminal Ready and Request-to-Send lines are inactive until initialized by the processor.
- Initializes the baud rate clock dividers (U13) to ensure proper timing synchronization.
- Interrupts the Z-80A CPU through its non-maskable interrupt (NMI) line. Note that during power-up when RESET is active, the RESET input is recognized by the Z-80A, and the NMI input is ignored.

Shared Memory Controller

Addressing

Communication between the card and mainframe is handled through a set of memory addresses, some of which are handled as registers. Only alternate addresses from the mainframe are used because the least-significant bit is not connected (shared address bit 0 is connected to mainframe address bit 1, etc.). The upper 2 bits of the shared address bus (shared address bits 13 and 14, mainframe address bits 14 and 15) determine the data destination (write) or source (read) as follows:

SA14	SA13	Source/Destination
0	0	Hardware Registers
0	1	RAM Lower Block (U25)
1	0	RAM Upper Block (U26)
1	1	Not used

Shared Memory addressing is accessed through a set of dual-input multiplexer/latch circuits (U39-42). The Access Select flip-flop (U19 pin 9) selects the memory address from the mainframe or interface CPU, then latches the address (U16 pin 3) to maintain proper signals during the memory cycle.

Read/Write Control

The mainframe read/write control line is buffered through the same multiplexer/latch circuits that handle memory addresses. U39 pin 15 carries mainframe read/write control (U39 pin 2) during mainframe memory accesses, and is held inactive during Z-80A accesses (U39 pin 3). The latched mainframe read/write signal controls the direction of the 8-bit bus transceiver (only the lower 8 bits of the 16-bit bus are used), and drives the 2B (read/write) input of the memory control multiplexer (U32).

The Z-80A read/write control line (ZRD) controls the direction of the shared data bus transceiver (U45), and drives the 2A (read/write) input of the memory control multiplexer (U32 pin 5). The Access Select flip-flop determines which input (2A or 2B) is used to drive the shared read (SRD) output which, when gated with shared memory timing clocks from U17, controls the RAM write enable (SWR) line.

Clock Circuits

The 7.3728 MHz oscillator drives a pair of flip-flop frequency dividers (U19 pins 1-6 and U15 pins 1-6) to generate symmetrical timing pulses at 1/2 and 1/4 the clock frequency, respectively. The 3.6864 MHz System Clock output (TP5) is also used to drive the Z-80A clock input after being waveshaped by Q1, Q2, and their associated circuitry. The output of the second divider (U15 pin 6) produces a 1.8432 MHz frequency reference for the CTC chip which generates baud rate timing signals for the SIO chip. CTC timing signals are fed to the SIO chip through the baud rate multiplexer (U11).

Memory Access Select Timing

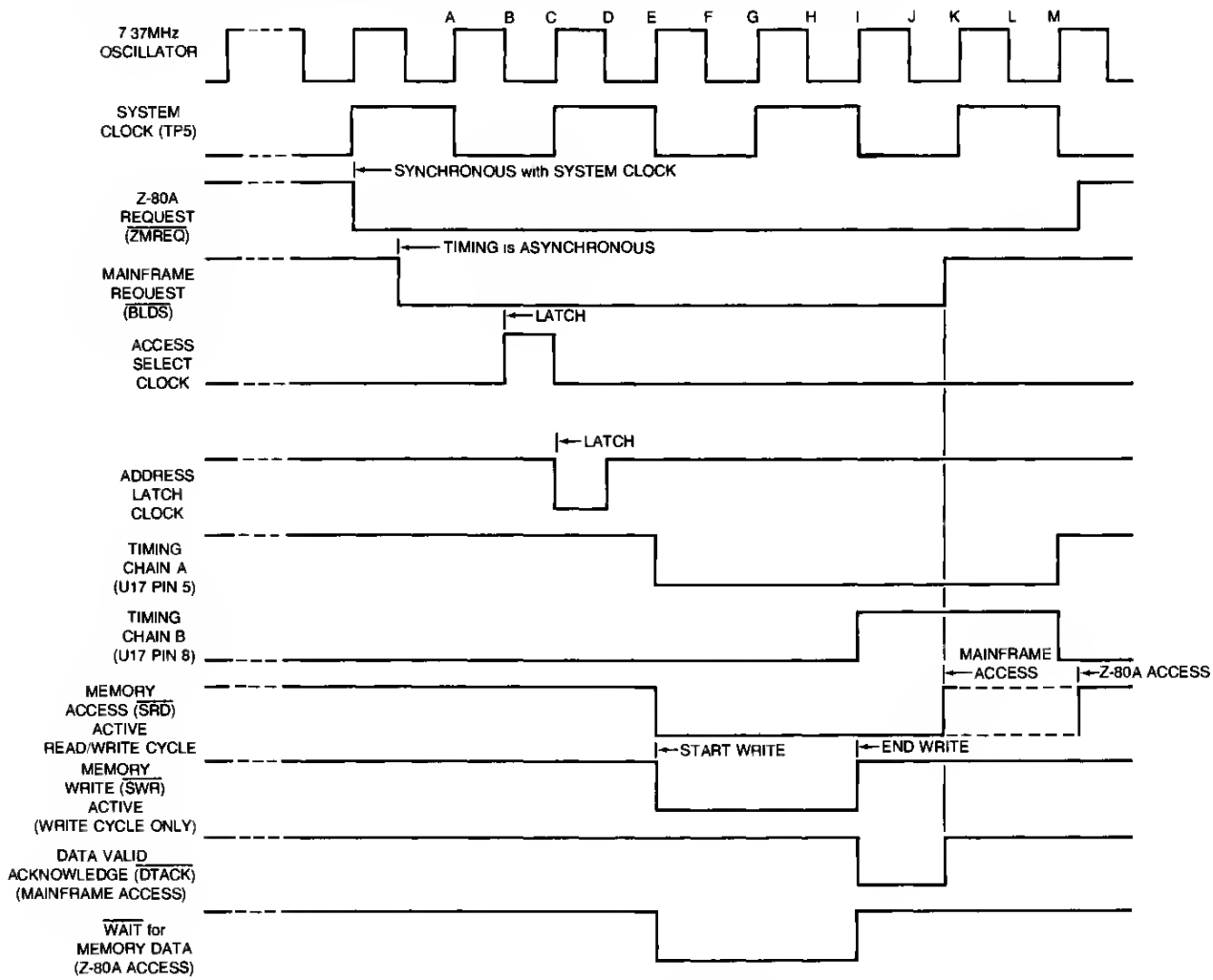
At the beginning of a processor memory cycle, the interface or mainframe CPU sends a memory request. The Z-80A outputs: A15, MREQ, and RFSH are combined (U24 pin 1) to drive the 1A input of the memory control multiplexer (U32). The mainframe BLDS output is combined with MYPA (TP6), then gated with shared memory timing (U17 pin 6 through U23 to U4 pin 11) to drive the 1B input of the memory control multiplexer (32). The same line is also connected to the D input of the Access Control flip-flop which selects the mainframe or interface processor when its clock line goes high.

The Access Control flip-flop is clocked when the oscillator and system clock (TP5) are both low (U24 pin 13 goes high). (Note that U16 pin 4 and U17 pin 6 are both low indicating that no memory cycle is in progress.) The state of the Access Select flip-flop's D input at clock time determines which processor gets control of the shared memory cycle. If D is low, the mainframe processor is connected; if D is high, access defaults to the Z-80A interface processor. When the System Clock (TP5) input to the timing chain goes high, the 1A or 1B input to the memory control multiplexer (U32) is selected by the Access Control flip-flop, inverted by the multiplexer, then used to start a memory cycle when the timing chain flip-flops (U17 pin 2) are clocked on the falling edge of the system clock (TP5).

Memory Cycle Timing

If no memory cycle is in progress, the shared memory access request lines from both processors are sampled on alternate falling edges of the 7.37 MHz clock when TP5 is LOW. If a memory cycle is in progress, request sampling is held off until the cycle is complete. The two memory cycle timing chain flip-flops (U17) control memory cycle timing.

Here is an explanation of a typical memory access cycle. The following timing diagram shows the relationship of the clock oscillator (U18) and the System Clock (TP5):


A B C D E F G H I J K L M
7.37MHz OSCILLATOR
SYSTEM CLOCK (TP5)
SYNCHRONOUS with SYSTEM CLOCK
Z-80A REQUEST (ZMREQ)
TIMING is ASYNCHRONOUS
MAINFRAME REQUEST (BLDS)
LATCH
ACCESS SELECT CLOCK
LATCH
ADDRESS LATCH CLOCK
TIMING CHAIN A (U17 PIN 5)
TIMING CHAIN B (U17 PIN 8)
MAINFRAME ACCESS
Z-80A ACCESS
MEMORY ACCESS (SRD) ACTIVE READ/WRITE CYCLE
START WRITE
END WRITE
MEMORY WRITE (SWR) ACTIVE (WRITE CYCLE ONLY)
DATA VALID ACKNOWLEDGE (DTACK) (MAINFRAME ACCESS)
WAIT for MEMORY DATA (Z-80A ACCESS)

Memory Cycle Timing Diagram

Assume that all previous memory cycles have run to completion. The Shared Memory Controller samples the incoming memory request lines on alternate falling edges of the clock oscillator when the System Clock at TP5 is LOW. When a shared memory access request is received, it propogates through intermediate gates and the memory control multiplexer (U32) then arrives asynchronously at the D input of the first timing chain flip-flop (U17 pin 2). If the request is from the mainframe, it arrives at the Access Select flip-flop's D input slightly earlier. (If a memory cycle is in progress, the access request from either processor is held off by U23 pins 3 and 14 which are held high by U17 pin 6. Both inputs go low at the end of the memory cycle, enabling any pending requests in order of established priority: mainframe takes precedence in simultaneous requests pending.)

When TP5 is LOW, if a shared memory request is pending prior to the falling edge (B) of the clock oscillator, the Access Select flip-flop is clocked to determine which processor gets control of shared memory. The output of the flip-flop is then sent to the various multiplexers that control signal routing in the memory and hardware register circuitry.

After the multiplexers have had time to settle, the address latches (U39-42) are clocked on the next rising edge (C) of the clock oscillator (TP5 also goes high). The latched address then propogates to the RAMs and hardware register address decoding circuits.

On the next falling edge of the system clock (TP5) which is also the next rising edge of the clock oscillator (E), the shared memory request at the D input of the first timing chain flip-flop is clocked causing the flip-flop to clear. The output change (Q output goes low) immediately disables clocking to the Access Select flip-flop and address multiplexer latches, and releases the Z-80A WAIT line if the Z-80A is selected. The 3Y or 4Y outputs of the memory control multiplexer (U32) are set to enable the appropriate data bus transceiver (U44 or U45), and the shared write control line (SWR) is gated to RAM (U36 pins 4 & 5 both high). This sequence initiates a memory read or write cycle.

The memory access (read or write) is complete on the next falling edge (I) of the system clock (TP5). At this time, the second timing chain flip-flop is clocked, causing pin 8 to go low. This disables the SWR line forcing it high (end of write cycle), and sends a DTACK (data acknowledge) to the mainframe if the mainframe has access to shared memory. The controller then hangs in the same state until the shared memory access request is removed by the processor. When the processor releases the request line, the D input (U17 pin 2) goes high, releasing the data bus transceivers. The timing chain then resets to its idle state. After the next rising clock edge to U17 pin 3, the controller is ready to process a new memory request.

Hardware Registers

The four read and four write registers that are implemented completely in hardware (RAM is not used) are selected when SA2 thru SA14 are all 0 (U36 pin 8 LOW). The hardware register decoder (U21) combines SA0, SA1, and the shared read line to enable the appropriate register.

Only bit 7 is implemented in write registers 0 and 1. Register 0, interface reset, sets the Reset flip-flop (U15 pins 8 thru 13). Register 1, interrupt enable, sets or clears the Interrupt Enable flip-flop (U14 pins 1 thru 6).

The upper nibble (bits 4 thru 7) of read registers 0 and 1 are implemented by the tri-state multiplexer (U33). SD0 thru SD3 are held high (0) by pullup resistors, except that SD2 is pulled low (1) by U33 pin 3 during reads from register 0 (interface ID). Read register 0 provides the Switch R setting (SW2 pin 8) and card identification to the shared data bus. Read register 1 provides the interrupt level switch settings, state of the interrupt request flip-flop, and the state of the interrupt enable flip-flop

Register 2 is the modem control and status register. Data written to this register is latched by the modem control latch (U6). Data inputs are taken from the modem status register buffer (U5).

Register 3 controls the hardware semaphore. Data inputs (read register) sample the state of the semaphore flip-flop (U14 pin 8). At the end of the read access, the flip-flop is clocked, causing the output to be set (D input is always 1). A write to this register clears the flip-flop by pulsing the clear line. The semaphore is normally used as hold-off flag to tell the other processor that a resource is in use and is not available until the current operation has been completed. At the end of the operation, the semaphore is cleared to enable access by the other processor. This provides a means to protect the integrity of circular shared data buffers and queues without risk of scrambling buffer and queue pointers and data.

Shared RAM

The two shared RAM sockets on the interface (U25 and U26) are designed to accept HP-approved 8-bit-wide static RAM chips. The sockets, if present, use 2 K-byte RAMs, but can accept 8 K-byte RAMs when they become available in the future. The sockets (or IC mounting holes) can accept 24 or 28-pin packages, but both must have the same size RAM installed. 24-pin RAM devices must be installed so that pins 1, 2, 27, and 28 are empty. Jumper wires must be properly configured to match the requirements of the RAM devices that are installed. W4 is used for 24-pin 2K x 8 RAMs; W3 is omitted.

RAM address space is divided into two segments: lower and upper blocks. The first two locations of the lower block are also connected to special decoding hardware that control interrupts between the processors that share the memory. One register is used as a command register; the other as an Interrupt Cause register. When commands are sent to the interface Command Register from the mainframe, the command flip-flop is set, causing an interrupt to the interface processor (if it is properly programmed) through the SIO CTSB input. Data placed in the Interrupt Cause register by the interface processor sets the Interrupt Request flip-flop which then interrupts the mainframe processor if interrupts are enabled.

Control and status communication between the mainframe and interface processors are handled thorugh the Interrupt Cause Register, Command Register, and Data Register. Communication sequences are as follows:

Mainframe Command to Interface:

1. Mainframe places new Control register value in Data Register (control operations only) then places Control or Status register number in Command Register. Command Register access sets interrupt request to Z-80A.
2. If Z-80A interrupt is enabled through SIO channel B (CTSB), the Z-80A responds to the interrupt, reads and stores the Data Register, reads and clears the Command Register value to zero, clears the interrupt, then transfers the Data Register value, if any, to the specified destination.
3. If the command is a status request, the status information is retrieved and placed in the Data Register where it is available to the mainframe.

Interface Interrupt to Mainframe:

1. Interrupt conditions are defined through a previous Control command to the interface. When any of those conditions is encountered, the interface processor places the interrupt cause in the Interrupt Cause register and sets the interrupt request flip-flop.
2. The mainframe responds to the interrupt if interrupts are enabled, and reads the Interrupt Cause register. If the register is zero, the interrupt is terminated. Otherwise, the mainframe processes every interrupt cause in the register, then exits the interrupt service process.

Default Switches

Default switches are normally used to define power-up default operating parameters. They are read, 4 at a time, by selecting which group is to be read through the 4-bit multiplexer (U20). ZA0 selects between upper and lower nibble, and the multiplexer output is enabled when both ZA5 and ZIORQ are both low. Switch functions are defined by interface card firmware.

Baud Rate Multiplexer

The baud rate multiplexer (U11) is controlled by the modem control latch. It can select from an external clock source through one of the line receivers, or it can select one of the timing outputs from the CTC chip. The selected clock source is then sent to the SIO chip to be used as a timing reference for received and transmitted data. Outputs are permanently enabled by grounding the enable inputs.

Line Drivers and Receivers

The interface has two types of line drivers: unbalanced and balanced. The unbalanced drivers are compatible with EIA RS-232C (CCITT V.28) and RS 423 (CCITT V.10) electrical interface standards. Driver rise and fall times are determined by the resistor connected to pin 1 of each driver package (U1, U2, U3, and U7). The 1-MΩ resistor on control signal drivers limits the rise time to approximately 100 μs. The data and clock drivers (U3) use a 20-KΩ resistor to reduce the rise time to about 2.2 μs. No-load output voltage should be +5 to 6 volts (ON) or −5 to 6 volts (OFF).

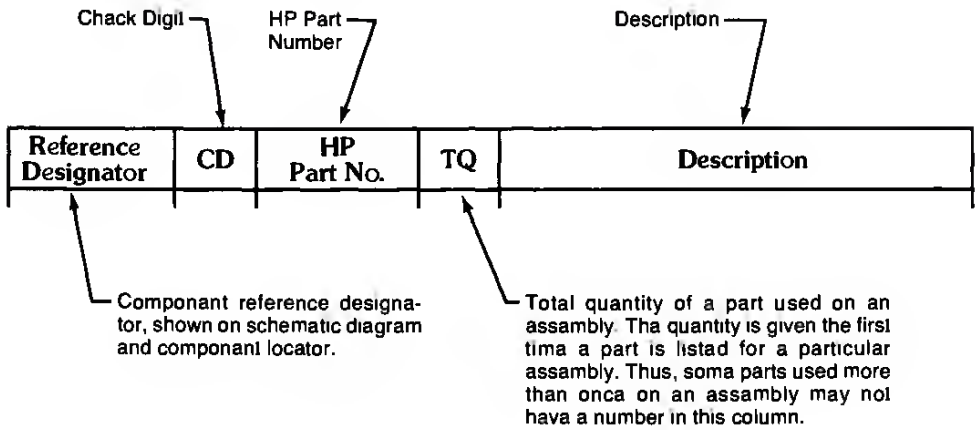
The balanced drivers (U8) implement the EIA RS-422 (CCITT V.11) electrical interface standard. The output levels of these drivers (measured to signal ground) should be between 0 and +5 volts.

The line receivers (U9 and U10) convert incoming RS-232, RS423, and RS422 signals to TTL-compatible levels. For unbalanced (RS-232 and RS423) connections, the non-inverting inputs are connected to signal ground in the cable connector at the interface rear panel. The incoming unbalanced signal lines are connected to the inverting receiver inputs. To ensure that open cable connections are interpreted as OFF, the non-inverting inputs are connected through 6-kΩ resistors to ground, while the inverting inputs are returned through 6-kΩ resistors to −2.37 volts.

RS-422 implementation requires that 100-Ω resistors be installed between inputs on all balanced receivers (CS, RD, and ST inputs) to match the line impedance of the incoming signal cable pairs. The 6-kΩ resistors need not be removed in such cases. Note that HP does not supply RS-422 cables and accessories for this interface.

Replacement Parts

The following parts list identifies HP part numbers and manufacturers' part numbers for component-level repairs by qualified personnel.


Chack Digit
HP Part Number
Description
Reference Designator
CD
HP Part No.
TQ
Description
Componant reference designator, shown on schematic diagram and componant locator.
Total quantity of a part used on an assambly. Tha quantity is given the first tima a part is listad for a particular assambly. Thus, soma parts used more than onca on an assambly may not hava a number in this column.

Replacement parts are available from Hewlett-Packard at the following address:

Corporate Parts Center
Hewlett-Packard Company
333 Logue Avenue
Mountain View, California 94042
Telephone: (415) 968-9200

Manufacturer code and part number are listed in the right-hand columns of the parts list. Manufacturers are as follows:

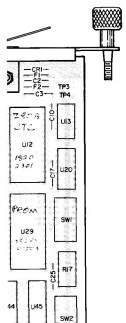
Mfr. No.	Manufacturer Name	Address		Zip Code
00000	Any satisfactory supplier			
01121	Allen-Bradley Co.	Milwaukee	WI	53204
01295	Texas Instr Inc Semicond Cmpnt Div.	Dallas	TX	75222
07263	Fairchild Semiconductor Div.	Mountain View	CA	94042
11236	CTS of Berne Inc.	Berne	IN	46711
24546	Corning Glass Works (Bradford)	Bradford	PA	16701
28480	Hewlett-Packard Co. Corporate Hq	Palo Alto	CA	94304
56289	Sprague Electric Co.	North Adams	MA	01247
91506	Augat Inc.	Attleboro	MA	02703
S4013	Hitachi	Tokyo, Japan		

Table 4-1. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	98628-66503	5	1	PC BOARD ASSEMBLY	28480	98628-66503
C1	0160-3487	8	22	CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3487
C2	0160-3487	8		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3487
C3	0180-0197	8	1	CAPACITOR-FXD 2.2UF +-10% 20VDC TA	56289	150D225X9020A2
C4	0160-3487	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3487
C5	0160-3487	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3487
C6	0160-3487	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3487
C7	0160-3487	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3487
C8	0180-1746	5	1	CAPACITOR-FXD 15UF +-10% 20VDC TA	56289	150D156X9020B2
C9	0180-0393	6	1	CAPACITOR-FXD 39UF +-10% 10VDC TA	56289	150D396X9010B2
C10	0160-3487	8		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3487
C12	0160-3487	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3487
C13	0160-3487	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3487
C14	0160-3487	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3487
C15	0160-4807	3	1	CAPACITOR-FXD 33PF +-5% 100VDC CER 0+-30	28480	0180-4807
C18	0160-3487	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3487
C17	0160-3487	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3487
C18	0160-3487	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3487
C19	0160-3487	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3487
C20	0160-3487	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3487
C21	0160-3487	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3487
C22	0160-3487	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3487
C23	0160-3487	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3487
C24	0160-3487	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3487
C25	0160-3487	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3487
C26	0160-3487	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3487
C27	0160-3487	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3487
CR1	1901-0025	2	1	DIODE-GEN PRP 100V 200MA DO-7	28480	1901-0025
CR2	1902-3002	3	1	DIODE-ZNR 2.37V 5% DO-7 PD=.4W TC=-.074%	28480	1902-3002
CR3	1901-0518	8	2	DIODE-SM SIG SCHOTTKY	28480	1901-0518
CR4	1901-0518	8		DIODE-SM SIG SCHOTTKY	28480	1901-0518
F1	2110-0297	4	1	FUSE .5A 125V NTD .281X.093	28480	2110-0297
F2	2110-0423	8	1	FUSE 1.5A 125V NTD .281X.093	28480	2110-0423
F3	2110-0592	2	1	FUSE 4A 125V NTD .281X.093	28480	2110-0592
Q1	1854-0019	3	1	TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0019
Q2	1853-0015	7	1	TRANSISTOR PNP SI PD=200MW FT=500MHZ	28480	1853-0015
R1	0683-1055	5	3	RESISTOR 1M 5% .25W CF TC=0-800	28480	0683-1055
R2	0683-1055	5		RESISTOR 1M 5% .25W CF TC=0-800	28480	0683-1055
R3	0757-0449	6	1	RESISTOR 20K 1% .125W F TC=0+-100	24546	CT4-1/8-TO-20D2-F
R4	0683-1055	5		RESISTOR 1M 5% .25W CF TC=0-800	28480	0683-1055
R5	0698-0082	7	4	RESISTOR 464 1% .125W F TC=0+-100	24546	CT4-1/8-TO-4640-F
R6	0757-0405	4	1	RESISTOR 162 1% .125W F TC=0+-100	24546	C4-1/8-TD-162R-F
R7	0698-0082	7		RESISTOR 464 1% .125W F TC=0+-100	24546	CT4-1/8-TO-4640-F
R8	0698-0082	7		RESISTOR 464 1% .125W F TC=0+-100	24546	CT4-1/8-TO-4640-F
R9	0698-0082	7		RESISTOR 464 1% .125W F TC=0+-100	24546	CT4-1/8-TO-4640-F
R10	0757-0346	2	2	RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-TD-10R0-F
R11	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-TD-10R0-F
R12	0698-0083	8	2	RESISTOR 1.96K 1% .125W F TC=0+-100	24546	C4-1/8-TD-1961-F
R13	0698-0083	8		RESISTOR 1.96K 1% .125W F TC=0+-100	24546	C4-1/8-TD-1961-F
R14	1810-0561	8	1	NETWORK-RES 16-DIP6.8K OHM X 15	28480	1810-0561
R15	1810-0517	4	2	NETWORK-RES 10-SIP6.0K OHM X 9	28480	1810-0517
R16	1810-0517	4		NETWORK-RES 10-SIP6.0K OHM X 9	28480	1810-0517
R17	1810-0162	5	1	NETWORK-RES 14-DIP4.7K OHM X 13	11236	760-1-R4.7K
SW1	3101-2510	0	2	SWITCH ASSEMBLY-ROCKER	28480	3101-2510
SW2	3101-2510	0		SWITCH ASSEMBLY-ROCKER	28480	3101-2510
U1	1820-2117	5	4	IC DRVR TTL LINE DRVR DUAL	07263	9636ATC
U2	1820-2117	5		IC DRVR TTL LINE DRVR DUAL	07263	9636ATC
U3	1820-2117	5		IC DRVR TTL LINE DRVR DUAL	07263	9636ATC
U4	1820-1201	6	1	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U5	1820-1491	6	1	IC BFR TTL LS NON-INV HEX 1-INP	01295	SN74LS367AN
U6	1820-1997	7	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U7	1820-2117	5		IC DRVR TTL LINE DRVR DUAL	07263	9636ATC
U8	1820-2703	5	1	IC DRVR TTL DIFF LINE DUAD	24840	1820-27D3
U9	1820-2594	2	2	IC RCVR TTL LS LINE RCVR QUAD 2-INP	24640	1820-2594
U10	1820-2594	2		IC RCVR TTL LS LINE RCVR QUAD 2-INP	24640	1820-2594

Table 4-1. Replaceable Parts (continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U11	1820-1244	7	1	IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS153N
U12	1820-2301	9	1	IC-Z80A CTC	28480	1820-2301
U13	1820-1112	8	3	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U14	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U15	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U16	1820-2657	8	2	IC GATE TTL ALS OR QUAD 2-INP	01295	SN74ALS32N
U17	1820-0693	8	2	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74AN
U18	1813-0225	7	1	CRYSTAL-CLOCK-OSCILLATOR	28480	1813-0225
U19	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74AN
U20	1820-1438	1	2	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS257AN
U21	1820-1245	8	2	IC DCDR TTL LS 2-TO-4-LINE DUAL 2-INP	01295	SN74LS155N
U22	1820-1245	8		IC DCDR TTL LS 2-TO-4-LINE DUAL 2-INP	01295	SN74LS155N
U23	1820-1440	5	1	IC LCH TTL LS QUAD	01295	SN74LS279N
U24	1820-2739	7	1	IC GATE TTL ALS NOR QUAD 2-INP	01295	SN74ALS02N
U25	1818-1611	7	1	IC	54013	HM6116P-3
U27	1820-2300	8	1	IC-Z80A SIO/2	28480	1820-2300
U28	1820-2298	3	1	IC-Z80A CPU	28480	1820-2298
	1200-0817	4	1	SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0817
U29	98628-81002	1	1	ROM	28480	98628-81002/81003
	1200-0861	5	1	SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0861
U30	1820-1199	1	1	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U31	1820-1281	2	1	IC DCDR TTL LS 2-TO-4-LINE DUAL 2-INP	01295	SN74LS139N
U32	1820-1428	9	1	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
U33	1820-1438	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS257AN
U34	1820-1427	8	1	IC DCDR TTL LS 2-TO-4-LINE DUAL 2-INP	01295	SN74LS156N
U35	1820-1568	8	1	IC BFR TTL LS BUS QUAD	01295	SN74LS125AN
U36	1820-1202	7	1	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
U37	1820-2657	8		IC GATE TTL ALS OR QUAD 2-INP	01295	SN74ALS32N
U38	1820-1905	7	1	IC GATE TTL LS NOR DUAL 5-INP	07263	74LS260PC
U39	1820-1444	9	4	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS298N
U40	1820-1444	9		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS298N
U41	1820-1444	9		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS298N
U42	1820-1444	9		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS298N
U43	1820-2740	0	1	IC COMPTR TTL LS MAGTO 2-INP 8-BIT	01295	SN74LS688N
U44	1820-2206	3	2	IC MISC TTL LS	01295	SN74LS640N
U45	1820-2206	3		IC MISC TTL LS	01295	SN74LS640N
W1	1258-0124	7	3	PIN-PROGRAMING JUMPER .30 CONTACT	91506	8136-475G1
	1200-0455	6	4	SOCKET-IC 8-CONT DIP-SLDR	28480	1200-0455
W2	1258-0124	7		PIN-PROGRAMING JUMPER .30 CONTACT	91506	8136-475G1
	1200-0455	6		SOCKET-IC 8-CONT DIP-SLDR	28480	1200-0455
	1200-0455	6		SOCKET-IC 8-CONT DIP-SLDR	28480	1200-0455
W4	1258-0124	7		PIN-PROGRAMING JUMPER .30 CONTACT	91506	8136-475G1
	1200-0455	6		SOCKET-IC 8-CONT DIP-SLDR	28480	1200-0455
				MISCELLANEOUS		
	0380-1324	9	2	STANDOFF-THO	28480	0380-1324
	0515-0145	7	2	SCREW-MACH M3 X 0.5 8MM-LG 90-DEG-FLH-HD	00000	ORDER BY DESCRIPTION
	1251-2248	6	2	LOCK SPRING-MICRO RBN CONN	28480	1251-2248
	1251-7119	0	2	END DISK-LATCH	28480	1251-7119
	1251-7161	2	1	CONNECTOR-50 POST RING	28480	1251-7161
	2380-0001	9	2	SCREW-MACH 6-32 .25-IN-LG FIL-HD-SLT	00000	ORDER BY DESCRIPTION
	7101-0612	3	1	I/O COVER	28480	7101-0612
	7121-1909	5	1	PC BOARD LABEL	28480	7121-1909
	09826-90021	6	1	MANUAL-DATA COMM	28480	09826-90021
	1251-6624	0	1	CONNECTOR-STD. TEST	28480	1251-6624
	1251-6625	1	1	TEST CONNECTOR (OPT. 001)	28480	1251-6625
	5061-4215	2	1	CABLE-DTE INTERFACE (FEMALE CONNECTOR)	28480	5061-4215
	5061-4216	3	1	CABLE-DCE INTERFACE (MALE CONNECTOR)	28480	5061-4216
	7121-1957	3	1	LABEL-SELECT CODE	28480	7121-1957



SSEMBLY OR SUB-

TED.

L A STRAIGHT LINE

HANGE INPUTS TO
LLING JUMPERS TO
O +5V AND INSTALL

$\frac{E}{1} = 3.6864$ MHz

$\frac{E}{5} = 1.8432$ MHz

HEWLETT PACKARD

Fireside Networks Division
5000 Foothills Boulevard
Roseville, California 95678

A1

DATA COMMUNICATIONS INTERFACE
SCHEMATIC DIAGRAM

Manual Part No. 98626-90000 & 98626-90001 | Dwg Rev. B | Sheet 1 of 1

Part No. 98628-90001

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